REMARKS

Claims 1-7 and 9-18 are rejected under 35 USC 103a as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217

Applicant asserts that claim 1 of the present invention should not be found rejected as being unpatentable over Kaku et al in view of Kato et al. because there are limitations of claim 1 that neither Kaku et al. nor Kato et al. teach.

MPEP section 2143 states the "Basic Requirements of a Prima Facie Case of Obviousness" for 35 USC 103 rejections as follows:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. **Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.**" (MPEP section 2143 – emphasis added)

Applicant points out that neither Kaku et al. nor Kato et al. teach at least the follow limitations found in claim 1 of the present invention:

> "the rough delay unit **for generating a fine delay parameter according to the selected set of write strategy parameters**, and for delaying the RLL modulation waveform according to the first clock signal and the selected set of write strategy parameters to generate a first delay signal; and"
>
> "the fine delay chain **for delaying the first delay signal according to the fine delay parameter so as to generate the write signal**, the fine delay chain having a plurality of serially connected delay cells, each delay cell delaying the first delay signal by a predetermined period;" (claim 1 of present

invention– emphasis added)

In particular, applicant points out that Fig.2 of Kaku et al. does not illustrate the delay circuit 114 generating a fine delay parameter. Instead, as explained in col 5, lines 47-50 state, "The write strategy control unit 104 includes a delay circuit 114 for realizing the write strategy control, according to which the recording pulse is generated depending upon the NRZ signal inputted, and a time position of the pulse and a pulse width thereof are adoptively and variable controlled". Col 7, lines 42-52 shed further light on the operation of the delay circuit 114 stating, "In the prior art, for bringing the timing of the NRZ modulation signal from the modulation circuit 7 into line with the reflection light, there is provided a delay circuit on the substrate. In the laser driver 10 according to the present invention, there can be obtained the NRZ modulation signal as well as the clock signal chCLK being synchronized therewith, and it is so constructed that the recording current signal can be generated corresponding to the NRZ signal through the delay circuit 114 disposed inside, and accordingly the delay circuit 114 is used for that purpose." Again, no mention of generating a fine delay signal according to the selected set of write strategy parameters is stated or suggested by Kaku et al. Additionally, Kaku et al. does not disclose a fine delay chain whatsoever.

Turning to Fig.3 of Kato et al., applicant points out that the rough delay 322 does not generate a fine delay signal according to a selected set of write strategy parameters for use by the fine delay 324 to thereby generate the write signal, as is claimed in claim 1 of the present invention. Instead, as is shown in Fig.3 and explained in col 5, lines 40-45, "Output delay control values N_1, and N_2 are fed to coarse and fine delays 322 and 324, respectively. Values N_1 and N_2 select the number of increments of coarse delay (1/4 T) and fine delay (1/32 T), respectively. Note that the resultant delay produced by course delay 322 and fine delay 324 will be the sum of the two delays" In other words, according to the teachings of Kato et al., the fine delay 324 delays the output of the rough delay 322 according to the output delay control value N_2, which is clearly shown in Fig.3 being generated by the write strategy delay

table 350 not the rough delay unit 322. Therefore, there is no fine delay signal generated by a rough delay unit according to a selected set of write strategy parameters that is utilized by a fine delay chain to delay a first delay signal outputted by the rough delay unit to thereby generate a write signal, as is claimed in claim 1 of the present invention. And the teachings of Kato et al. do not suggest such operation.

Because neither Kaku et al. nor Kato et al. teach or suggest all the limitations of claim 1 of the present invention, a combination of said references cannot teach all the limitations of claim 1 of the present invention. Therefore, applicant asserts that claim 1 should not be found rejected under 35 USC 103a as being unpatentable over Kaku et al. in view of Kato et al. Reconsideration of claim 1 is respectfully requested. As claims 4-18 are dependent on claim 1, if claim 1 is found allowable, so too should dependent claims 4-18.

Claim 8 is rejected under 35 USC 103a as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217 as applied to claim 3 above, and further in view of Chung et al., US Patent 4,873,680

As stated above, claim 8 is dependent on claim 1, which is believed by applicant to be allowable over the cited references. Therefore, claim 8 should also be found allowable over said cited references. Reconsideration of claim 8 is respectfully requested.

Sincerely yours,

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